

General Description

The GXN7426 combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. This device is ideal for load switch and battery protection applications.

RoHS and Halogen-Free Compliant

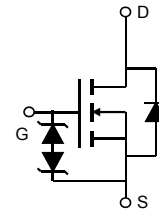
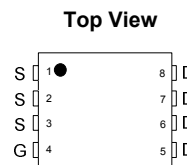
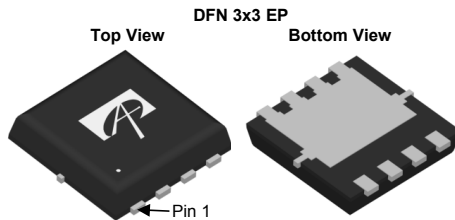
Product Summary

V_{DS}	30V
I_D (at $V_{GS}=10V$)	40A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	< 5.5m Ω
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	< 8m Ω

Typical ESD protection

HBM Class 3A

100% UIS Tested
100% R_g Tested



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^G	I_D	$T_C=25^\circ\text{C}$	A
		$T_C=100^\circ\text{C}$	
Pulsed Drain Current ^C	I_{DM}	130	A
Continuous Drain Current	I_{DSM}	$T_A=25^\circ\text{C}$	A
		$T_A=70^\circ\text{C}$	
Avalanche Current ^C	I_{AS}, I_{AR}	35	A
Avalanche energy $L=0.1\text{mH}$ ^C	E_{AS}, E_{AR}	61	mJ
Power Dissipation ^B	P_D	$T_C=25^\circ\text{C}$	W
		$T_C=100^\circ\text{C}$	
Power Dissipation ^A	P_{DSM}	$T_A=25^\circ\text{C}$	W
		$T_A=70^\circ\text{C}$	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	30	40	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^{A,D}		Steady-State	60	75
Maximum Junction-to-Case	$R_{\theta JC}$	3.5	4.2	$^\circ\text{C/W}$

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}, V_{GS}=0\text{V}$	30	36		V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=30\text{V}, V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			1 5	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}, V_{GS}=\pm 20\text{V}$			10	μA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1.35	1.85	2.35	V
$I_{D(ON)}$	On state drain current	$V_{GS}=10\text{V}, V_{DS}=5\text{V}$	130			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}, I_D=18\text{A}$ $T_J=125^\circ\text{C}$		4.5 7.2	5.5 8.8	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}, I_D=14\text{A}$		5.8	8	
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}, I_D=18\text{A}$		75		S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}, V_{GS}=0\text{V}$		0.7	1	V
I_S	Maximum Body-Diode Continuous Current				35	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}, V_{DS}=15\text{V}, f=1\text{MHz}$	1410	1765	2120	pF
C_{oss}	Output Capacitance		195	283	370	pF
C_{riss}	Reverse Transfer Capacitance		90	155	220	pF
R_g	Gate resistance	$V_{GS}=0\text{V}, V_{DS}=0\text{V}, f=1\text{MHz}$	1.3	2.6	3.9	Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}, V_{DS}=15\text{V}, I_D=18\text{A}$	26	33	40	nC
$Q_g(4.5\text{V})$	Total Gate Charge		12.5	16	19.5	nC
Q_{gs}	Gate Source Charge			5.2		nC
Q_{gd}	Gate Drain Charge			6.2		nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=10\text{V}, V_{DS}=15\text{V}, R_L=0.83\Omega,$ $R_{GEN}=3\Omega$		6		ns
t_r	Turn-On Rise Time			4		ns
$t_{D(off)}$	Turn-Off DelayTime			33		ns
t_f	Turn-Off Fall Time			7.5		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=18\text{A}, dI/dt=500\text{A}/\mu\text{s}$	9.5	12.3	15	ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=18\text{A}, dI/dt=500\text{A}/\mu\text{s}$	20	25	30	nC

- A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The Power dissipation P_{DSM} is based on $R_{\theta JA} t \leq 10\text{s}$ value and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design, and the maximum temperature of 150°C may be used if the PCB allows it.
- B. The power dissipation P_D is based on $T_{J(MAX)}=150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
- C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=150^\circ\text{C}$. Ratings are based on low frequency and duty cycles to keep initial $T_J=25^\circ\text{C}$.
- D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
- E. The static characteristics in Figures 1 to 6 are obtained using $<300\mu\text{s}$ pulses, duty cycle 0.5% max.
- F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}=150^\circ\text{C}$. The SOA curve provides a single pulse rating.
- G. The maximum current rating is package limited.
- H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

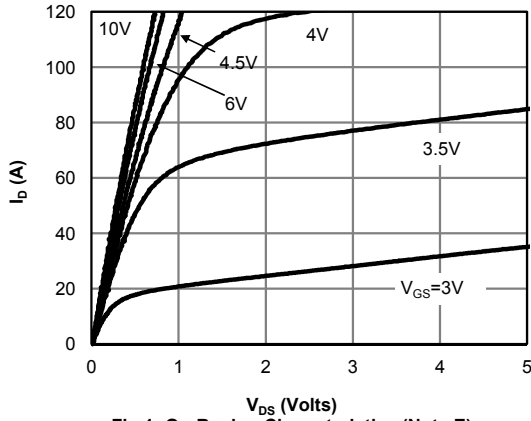


Fig 1: On-Region Characteristics (Note E)

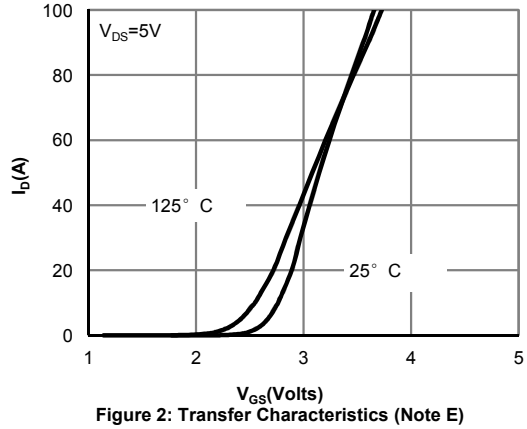


Figure 2: Transfer Characteristics (Note E)

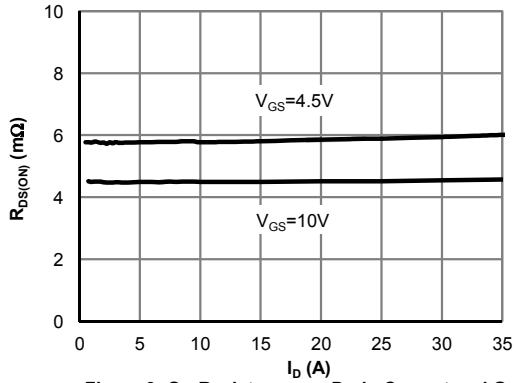


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

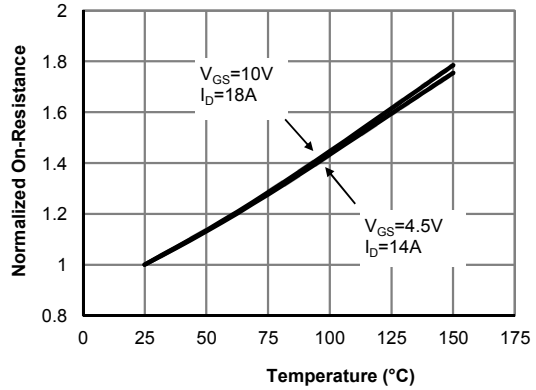


Figure 4: On-Resistance vs. Junction Temperature (Note E)

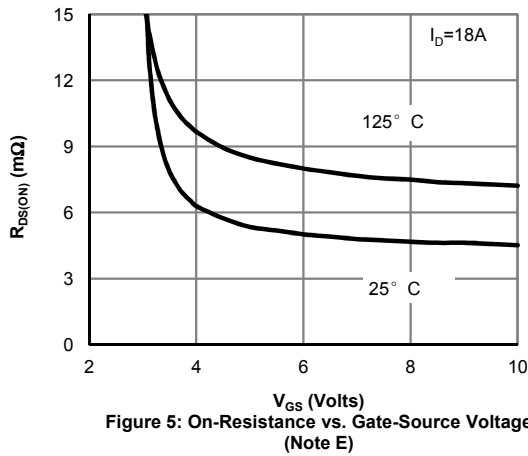


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

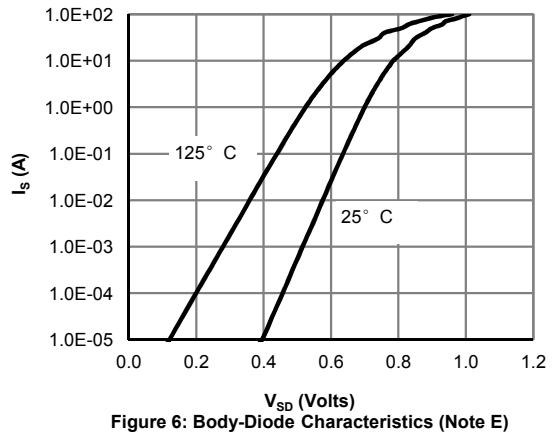


Figure 6: Body-Diode Characteristics (Note E)

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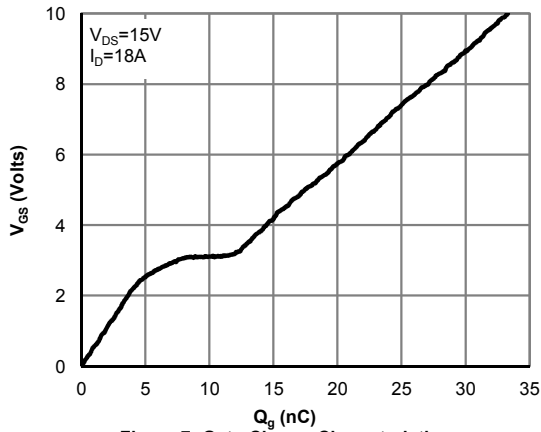


Figure 7: Gate-Charge Characteristics

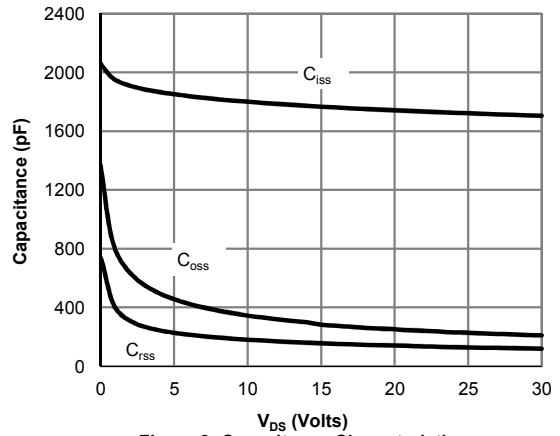


Figure 8: Capacitance Characteristics

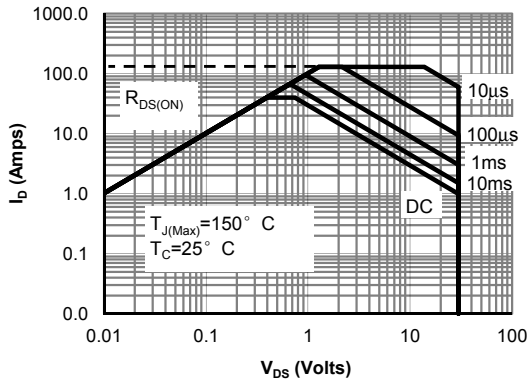


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

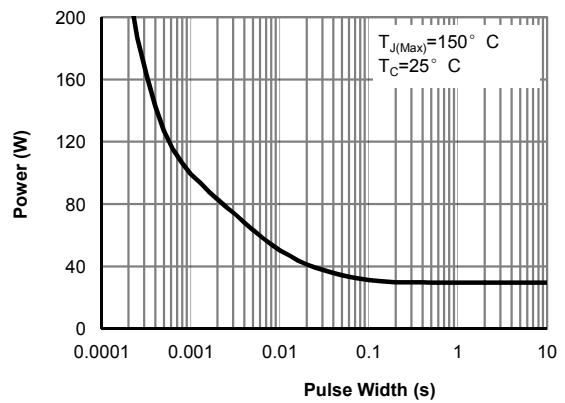


Figure 10: Single Pulse Power Rating Junction-to-Ca (Note F)

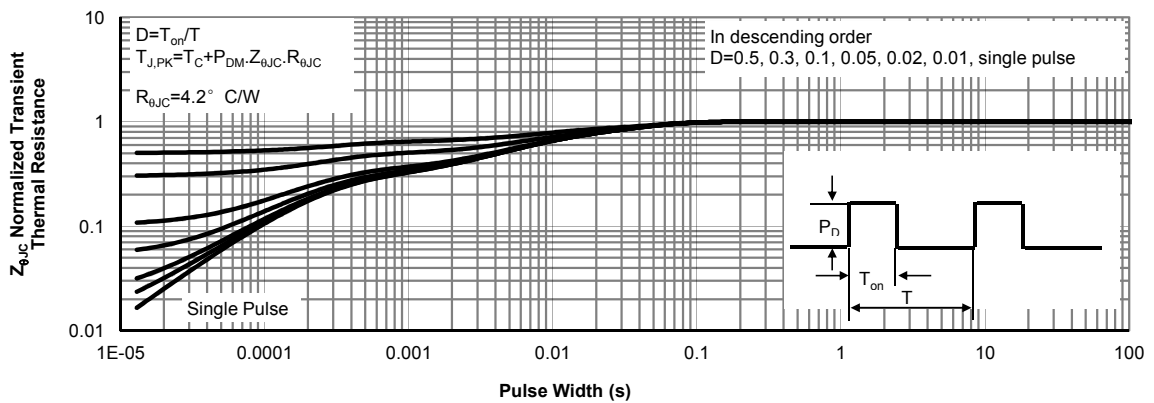


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

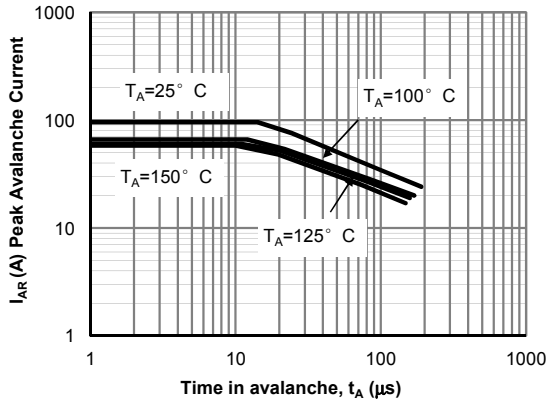


Figure 12: Single Pulse Avalanche capability (Note C)

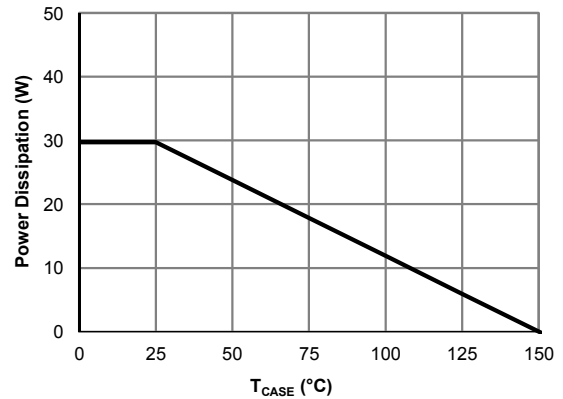


Figure 13: Power De-rating (Note F)

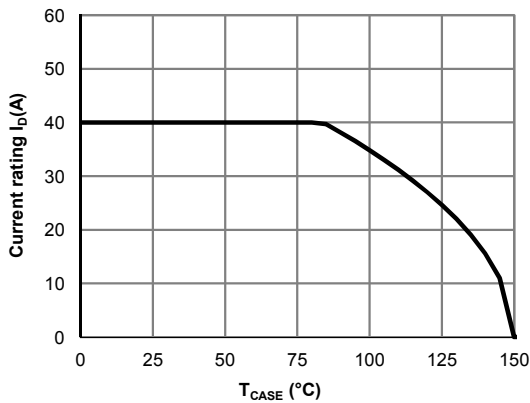


Figure 14: Current De-rating (Note F)

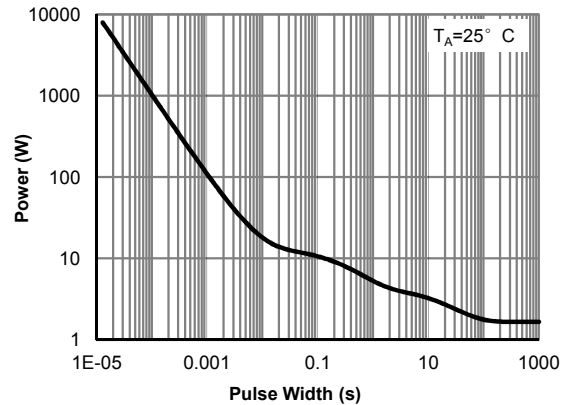


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

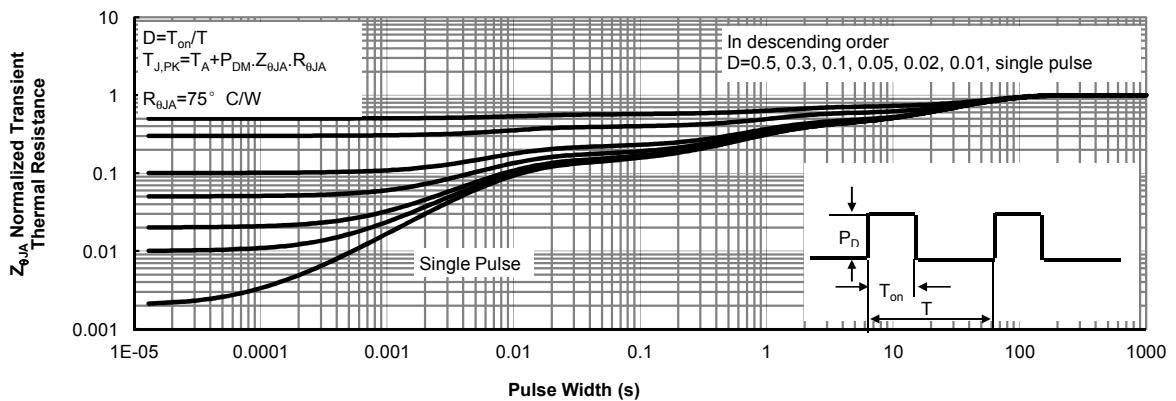
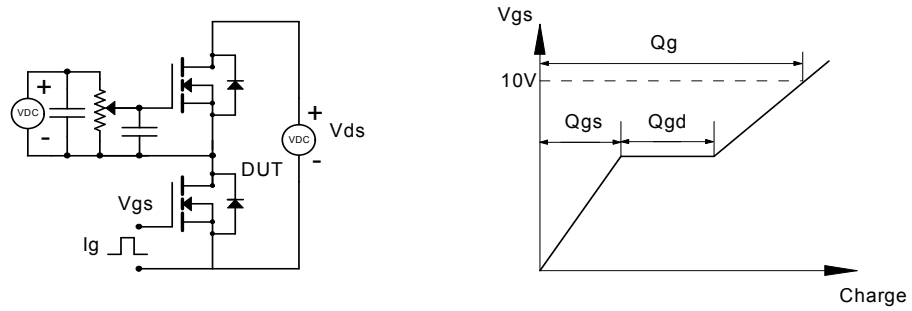
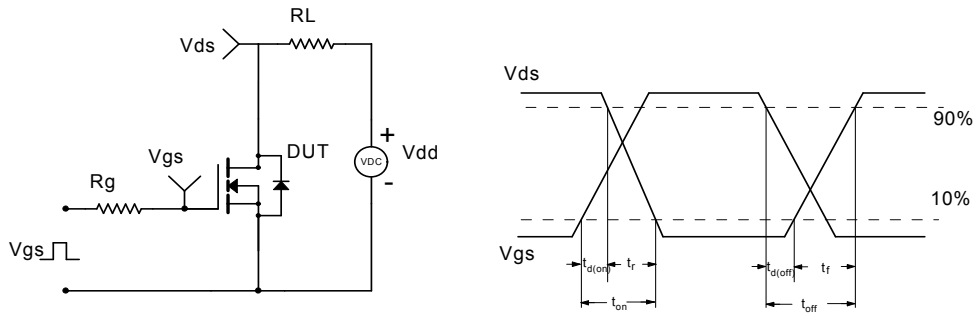


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

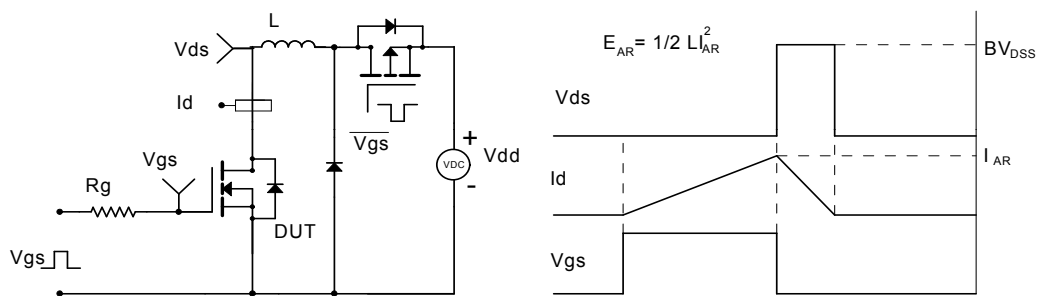
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

